History and overview of high performance computing

CPS343

Parallel and High Performance Computing

Spring 2020

CPS343 (Parallel and HPC) History and overview of high performance cor

Outline

I High-Performance Computing in the modern computing era

- 1940s-1960s: the first supercomputers
- 1975–1990: the Cray era
- 1990-2010: the cluster era
- 2000-present; the GPU and hybrid era

2 What does high performance computing look like today?

- Top Lists
- Grand Challenge Problems
- Parallelism
- Some things to think about

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The development of the modern supercomputer was largely driven by military needs.

- World War II
 - hand-computed artillery tables used during war; led to development in the USA of ENIAC (Electronic Numerical Integrator and Computer) from 1943 to 1946.
 - Nazi codes like Enigma were cracked in large part by machines Bombe and Colossus in the UK.
- Cold War
 - Nuclear weapon design
 - Aircraft, submarine, etc. design
 - Intelligence gathering and processing
 - Code breaking

ENIAC, 1943

The "Electronic Numerical Integrator and Computer" was the first storedprogram electronic computer.

Designed and built at the University of Pennsylvania from 1943 to 1946, it was transferred to Maryland in 1947 and remained in operation until 1955



Image source: http://ftp.arl.army.mil/ftp/historic-computers/gif/eniac3.gif

CDC 6600, 1964

The Control Data Corporation's CDC 6600 could do 500 KFLOP/s up to 1 MFLOP/s and was the first computer dubbed a "supercomputer."



Image source: http://en.wikipedia.org/wiki/File:CDC_6600.jc.jpg

ILLIAC-IV, 1966-1976

ILLIAC-IV was the forth Illinois Automatic Computer.



- design began in 1966; goal was 1 GFLOP/s and estimated cost was \$8 million
- "finished" in 1971-1972 at a cost of \$31 million and a top speed well below the 1 GFLOP/s goal
- designed to be a parallel computer with linear array of 256 64-bit processing elements, the final computer had only a fraction of this amount

Image source: http://en.wikipedia.org/wiki/File:ILLIAC_4_parallel_computer.jpg ***

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Cray 1, 1976

Seymour Cray, the architect of the 6600 and other CDC computers, started his own company, Cray Research Inc., in 1972.

Cray 1

- scalar and vector processor, 80 MHz clock, capable of 133 MFLOP/s for in normal use.
- \$5 to \$8 million
- 20-ton compressor for Freon cooling system
- shape facilitated shorter wire lengths, increasing clock speed



Image source: http://en.wikipedia.org/wiki/File:Cray-1-deutsches-museum.jpg

Cray X-MP (1982) and Y-MP (1988)

Cray X-MP

- 105 MHz
- two vector processors, each capable of 200 MFLOPS
- memory shared by all processors





• 167 MHz

- 2, 4, or 8 vector processors, each capable of 333 MFLOPS
- shared memory for all processors

Image sources: http://www.piggynap.com/awesome/cray-supercomputer-computing-in-the-80s/ and

http://www.flickr.com/photos/llnl/4886635870/

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- During the 1980s speed in supercomputers was primarily achieved through two mechanisms:
 - vector processors: these were designed using a *pipeline* architecture to rapidly perform a single floating point operation on a large amount of data. Achieving high performance depended on data arriving in the processing unit in an uninterrupted stream.
 - Shared memory multiprocessing: a small number (up to 8) processors with access to the same memory space. Interprocess communication took place via the shared memory.
- Cray was not the only player, other companies like Convex and Alliant marketed vector supercomputers during the 1980s.
- Some believed vector processing this was a better approach to HPC than using many smaller processors. Seymour Cray famously said 'If you were plowing a field, which would you rather use? Two strong oxen or 1024 chickens?'

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- The age of truly effective parallel computers had begun, but was already limited by access to shared memory.
- Memory contention was a major impediment to increasing speed; the vector processors required high-speed access to memory but multiple processors working simultaneously created contention for memory that reduced access speed.
- Vector processing worked well with 4 or 8 processors, but memory contention would prevent a 64 or 128 processor machine from working efficiently.

- The alternative to shared memory is *distributed memory*, where each processor has a dedicated memory space.
- The challenge became implementing effective processes communication – processes can't communicate with one another by writing data into shared memory; a *message* must be passed.
- During the 1980s there began to be a lot of interest in distributed memory computers.

Intel iPSC Hypercube, 1985

- between 32 and 128 nodes
- each node has
 - 80286 processor
 - 80287 math co-processor
 - 512K of RAM
 - 8 Ethernet ports (7 for other compute nodes, one for control node)
- used *hypercube* connection scheme between processors
- base model was 5-dimension hypercube (2⁵ = 32 processors)
- \bullet superseded by iPSC/2 in 1987



Image source: http://www.flickr.com/photos/carrierdetect/3599265588/

Thinking Machines' Connection Machines



- The CM-1 was a massively parallel computer with 65,536 SIMD processing elements arranged in a hypercube
- Each element was composed of a 1-bit processor and 4Kbits of RAM (the CM-2 upped this to 64 Kbits)
- CM-5, a MIMD computer with a different network topology, was at the top of the first Top 500 list in 1993. Located at Los Alamos National Lab, it had 1024 processors and was capable of 59.7 GFLOPS.

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http://www.computerhistory.org/revolution/supercomputers/10/73

Beowulf Clusters, 1994-present

- In 1994 Donald Becker and Tom Stirling, both at NASA, built a cluster using available PCs and networking hardware.
- 16 Intel 486DX PCs connected with 10 Mb/s Ethernet
- Achieved 1 GFLOP/s on \$50,000 system
- Named Beowulf by Stirling in reference to a quote in some translations of the epic poem *Beowulf* that says '*Because my heart is pure, I have the strength of a thousand men.*'



Image source: http://www.ligo.caltech.edu/LIG0_web/0203news/0203mit.html

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- During the 2000s the trend of increasing processor speeds was replaced with increasing the number of processor cores
- This led to hybrid clusters with a large number of processors, each with a small number of core sharing RAM and some cache space
- with the development of GPU and other general purpose accelerator hardware, today's top supercomputers are hybrid clusters with
 - a large number of standard processor nodes
 - each node has a multicore processor with some individual cache, some shared cache, and RAM shared by all cores
 - some number of GPU or other accelerators that are used for offloading specific types of computation from the CPU nodes
- Computation speed often limited by data-movement rate

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The Top 500 List

The site www.top500.org maintains a list of fastest computers in the world, according to a particular benchmark program. A new list comes out every June and November. As of the November 2019 the list starts with:

Rank	System	Cores	Rmax (TFlop/s)	Rpeak (TFlop/s)	Power (kW)
1	Summit - IBM Power System AC922, IBM POWER9 22C 3.076Hz, NVIDIA Volta GV100, Dual-rail Mellanox EDR Infiniband , IBM DoE/S/C/0Ak Idge National Laboratory United States	2,414,592	148,600.0	200,794.9	10,096
2	Sierra - IBM Power System AC922, IBM POWER9 22C 3.1GHz, NVIDIA Votta GV100, Dual-rail Metlanox EDR Infiniband , IBM / NVIDIA / Metlanox DOC/NNSA/LLNL United States	1,572,480	94,640.0	125,712.0	7,438
3	Sunway TaihuLight - Sunway MPP, Sunway SW26010 260C 1.45GHz, Sunway, NRCPC National Supercomputing Center in Wuxi China	10,649,600	93,014.6	125,435.9	15,371
4	Tianhe-2A - TH-IVB-FEP Cluster, Intel Xeon E5-2692v2 12C 2.26Hz, TH Express-2, Matrix-2000, NUDT National Super Computer Center in Guangzhou China	4,981,760	61,444.5	100,678.7	18,482
5	Frontera - Dell Có420, Xeon Platinum 8280 28C 2.76Hz, Mellanox InfiniBand HDR , Dell EMC Texas Advanced Computing Center/Univ. of Texas United States	448,448	23,516.4	38,745.9	
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#1 - 148.6 PFLOPs – Summit: IBM Power System AC922



- Location: Oak Ridge National Laboratory, Tennessee USA
- 4,608 compute nodes
- two IBM POWER9 processors and 512GB DDR4 RAM per node
- six NVIDIA Volta V100 GPUs with 640 Tensor cores, 5,120 CUDA cores, and 96GB HBM2 RAM per node
- Interconnect: Mellanox EDR 100G InfiniBand

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#2 – 94.6 PFLOPs – Sierra: IBM Power System AC922



- Location: Lawrence Livermore National Laboratory, California USA
- 4,320 compute nodes
- two IBM POWER9 processors with 256GB DDR4 RAM per node
- four NVIDIA Volta V100 GPUs with 640 Tensor cores, 5,120 CUDA cores, and 64GB HBM2 RAM per node
- Interconnect: Mellanox EDR 100G InfiniBand

Image source: https://media.datacenterdynamics.com/media/images/sierraLLNL_width_880.png 🖡 🗸 🚊 🦻 🚊

#3 – 93.0 PFLOPs – Sunway TaihuLight: Sunway MPP



- Location: National Supercomputing Center, Wuxi China
- Purpose: research and engineering work
- Cores: 10,649,600
- Memory: 1,310,720 GB
- Processor: Sunway SW26010 260C 1.45GHz
- Interconnect: Sunway

Image source: https://www.top500.org/static/featured/TaihuLight.jpg

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The benchmark used for the Top 500 list is the *High Performance LINPACK* (HPL) benchmark and is based on a variant of *LU* factorization with row partial pivoting. The main criticism of the HPL benchmark is that this problem is not representative of many important applications.

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A new benchmark, called the *High Performance Conjugate Gradients* (HPCG) benchmark (www.hpcg-benchmark.org), is an effort to create a new metric for ranking HPC systems and is intended as a complement to the High Performance LINPACK (HPL) benchmark.

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The HPCG benchmark is designed to exercise computational and data access patterns that more closely match a broad set of important applications, and to give incentive to computer system designers to invest in capabilities that will have impact on the collective performance of these applications.

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HPCG: a new benchmark

November 2019 HPCG Results from https://www.top500.org:

Rank	TOP500 Rank	System	Cores	Rmax (TFlop/s)	HPCG (TFlop/s)
1	1	Summit - IBM Power System AC922, IBM POWER9 22C 3.07GHz, NVIDIA Volta GV100, Dual-rail Mellanox EDR Infiniband , IBM DOE/SC/Oak Ridge National Laboratory United States	2,414,592	148,600.0	2925.75
2	2	Sierra - IBM Power System AC922, IBM POWER9 22C 3.1GHz, NVIDIA Volta GV100, Dual-rail Mellanox EDR Infiniband , IBM / NVIDIA / Mellanox DOE/NNSA/LLNL United States	1,572,480	94,640.0	1795.67
3	7	Trinity - Cray XC40, Xeon E5-2698v3 16C 2.3GHz, Intel Xeon Phi 7250 68C 1.4GHz, Aries interconnect , Cray/HPE D0E/NNSA/LANL/SNL United States	979,072	20,158.7	546.12
4	8	Al Bridging Cloud Infrastructure (ABCI) - PRIMERGY CX2570 M4, Xeon Gold 6148 20C 2.4GHz, NVIDIA Tesla V100 SXM2, Infiniband EDR , Fujitsu National Institute of Advanced Industrial Science and Technology (AIST) Japan	391,680	19,880.0	508.85
5	6	Piz Daint - Cray XC50, Xeon E5-2690v3 12C 2.6GHz, Aries interconnect , NVIDIA Tesla P100 , Cray/HPE Swiss National Supercomputing Centre [CSCS] Switzerland	387,872	21,230.0	496.98

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Supercomputers use a lot of power!

- Summit draws 10,096 kW and uses 88 GWh per year.
- Sierra draws 7,438 kW and uses 65 GWh per year.
- TaihuLight draws 15,371 kW and uses 135 GWh per year.

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- Sierra draws 7,438 kW and uses 65 GWh per year.
- TaihuLight draws 15,371 kW and uses 135 GWh per year.
- According to the U.S. Energy Information Administration, in 2018 the average U.S. home used 10,972 kWh of electricity per year.¹
- Summit uses enough energy to power 8,061 U.S. homes.
- TaihuLight needs about as much power as 12,272 U.S. homes!

http://www.eia.gov/tools/faqs/faq.cfm?id=97&t=3

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- Summit uses enough energy to power 8,061 U.S. homes.
- TaihuLight needs about as much power as 12,272 U.S. homes!
- Using \$0.12 per kWh, the cost of running Summit is just over **\$10.6** million per year; the annual cost for TaihuLight is over **\$16.1** million per year! This *does not include the cost of cooling...!*
- The *Massachusetts Green High Performance Computing Center* in Holyoke draws 10,000 kW, mostly hydroelectric power.

¹http://www.eia.gov/tools/faqs/faq.cfm?id=97&t=3. (B) (E) (CPS343 (Parallel and HPC) History and overview of high performance cor Spring 2020 27/49

The Green 500 List

It is becoming more common to talk about HPC systems in terms of their MFLOPs per watt as a measure of how efficient they are.

The top 5 of the November 2019 Top 500 list:

System	TFLOP/s	GFLOP/watt	Total power (kW)		
Summit (ORNL)	148,600	14.7187	10,096		
Sierra (LLNL)	94,640	12.7239	7,438		
TaihuLight (China)	93,015	6.0513	8,209		

The top 3 of the November 2019 Green 500 list:

System	TFLOP/s	GFLOP/watt	Total power (kW)
A64FX (Japan)	2,000	16.876	118
NA-1 (Japan)	1,303	16.265	80
AiMOS (RPI)	8,045	15.771	510

The Green 500 List

November 2019 Green500 Results from https://www.top500.org:

Rank	TOP500 Rank	System	Cores	Rmax (TFlop/s)	Power (kW)	Power Efficiency (GFlops/watts)
1	159	A64FX prototype - Fujitsu A64FX, Fujitsu A64FX 48C 2GHz, Tofu interconnect D , Fujitsu Fujitsu Numazu Plant Japan	36,864	1,999.5	118	16.876
2	420	NA-1 - ZettaScaler-2.2, Xeon D-1571 16C 1.3GHz, Infiniband EDR, PEZY-SC2 700Mhz , PEZY Computing / Exascaler Inc. PEZY Computing K.K. Japan	1,271,040	1,303.2	80	16.256
3	24	AiMOS - IBM Power System AC922, IBM POWER9 20C 3.45GHz, Dual-rail Mellanox EDR Infiniband, NVIDIA Volta GV100, IBM Rensselaer Polytechnic Institute Center for Computational Innovations [CCI] United States	130,000	8,045.0	510	15.771
4	373	Satori - IBM Power System AC922, IBM POWER9 20C 2.46Hz, Infiniband EDR, NVIDIA Tesla V100 SXM2, IBM MIT/MGHPCC Holyoke, MA United States	23,040	1,464.0	94	15.574
5	1	Summit - IBM Power System AC922, IBM POWER9 22C 3.070Hz, NVIDIA Volta GV100, Dual-rail Mellanox EDR Infiniband, IBM DOE/SC/Oak Ridge National Laboratory United States	2,414,592	148,600.0	10,096	14.719

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Grand Challenges

Quote from: National Science Foundation Advisory Committee for Cyberinfrastructure Task Force on Grand Challenges, Final Report, March 2011:

The "Grand Challenges" were U.S. policy terms set in the 1980's as goals for funding high-performance computing and communications research in response to foreign competition. They were described as "fundamental problems of science and engineering, with broad applications, whose solution would be enabled by high-performance computing resources..."

Today, the Grand Challenges are interpreted in a much broader sense with the realization that they cannot be solved by advances in HPC alone: they also require extraordinary breakthroughs in computational models, algorithms, data and visualization technologies, software, and collaborative organizations uniting diverse disciplines.

A (1) > A (2) > A

According to the NFS Grand Challenges final report, some of the important Grand Challenges are:

- Advanced New Materials
- Prediction of Climate Change
- Quantum Chromodynamics and Condensed Matter Theory
- Semiconductor Design and Manufacturing
- Assembling the Tree of Life
- Drug Design and Development
- Energy through Fusion
- Water Sustainability

- Understanding Biological Systems
- New Combustion Systems
- Astronomy and Cosmology
- Hazard Analysis and Management
- Human Sciences and Policy
- Virtual Product Design
- Cancer Detection and Therapy

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The following slides are shamelessly borrowed from Henry Neeman's presentation "What the heck is Supercomputing?" given at the NCIS sponsored *Introduction to Parallel and Cluster Computing* at Oklahoma University, summer 2012.

These slides use a simple metaphor to introduce several key issues (look for the **<u>bold underlined</u>** terms) in parallel computing that we will need to deal with during our course.



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Serial Computing



Suppose you want to do a jigsaw puzzle that has, say, a thousand pieces.

We can imagine that it'll take you a certain amount of time. Let's say that you can put the puzzle together in an hour.



NCSI Parallel & Cluster: Overview U Oklahoma, July 29 - Aug 4 2012



Shared Memory Parallelism

If Scott sits across the table from you, then he can work on his half of the puzzle and you can work on yours. Once in a while, you'll both reach into the pile of pieces at the same time (you'll *contend* for the same resource),

which will cause a little bit of slowdown. And from time to time you'll have to work together (<u>communicate</u>) at the interface between his half and yours. The speedup will be nearly 2-to-1: y'all might take 35 minutes instead of 30.



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The More the Merrier?

Now let's put Paul and Charlie on the other two sides of the table. Each of you can work on a part of the puzzle, but there'll be a lot more contention for the shared resource (the pile of puzzle pieces) and a lot more communication at the interfaces. So y'all will get noticeably less than a 4-to-1 speedup, but you'll still have an improvement, maybe something like 3-to-1: the four of you can get it done in 20 minutes instead of an hour.



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Diminishing Returns

If we now put Dave and Tom and Horst and Brandon on the corners of the table, there's going to be a whole lot of contention for the shared resource, and a lot of communication at the many interfaces. So the speedup y'all get will be much less than we'd like; you'll be lucky to get 5-to-1.

So we can see that adding more and more workers onto a shared resource is eventually going to have a diminishing return.



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More Distributed Processors



It's a lot easier to add more processors in distributed parallelism. But, you always have to be aware of the need to decompose the problem and to communicate among the processors. Also, as you add more processors, it may be harder to *load balance* the amount of work that each processor gets.





Load balancing means ensuring that everyone completes their workload at roughly the same time.

For example, if the jigsaw puzzle is half grass and half sky, then you can do the grass and Scott can do the sky, and then y'all only have to communicate at the horizon – and the amount of work that each of you does on your own is roughly equal. So you'll get pretty good speedup.



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- Making effective use of HPC takes quite a bit of effort; both learning how to use it and in developing software.
- It seems like a lot of trouble just to get code to run faster...
- Sure, it's nice to speed up code that normally runs for 24 hours so that it runs in 1 hour, but if you can afford to wait a day for the result, why bother with HPC?

In many cases, HPC is worth pursuing because

- HPC provides the ability (unavailable elsewhere) to solve bigger and more exciting problems: You can tackle bigger problems in the same amount of time and/or you can solve the same sized problems in less time.
- What happens in HPC today will be on your desktop (or in your pocket) in about 10 to 15 years people working in HPC are ahead of the curve!

A dividend of high performance computing...

And now for something completely different...

Question: What historically significant web application was developed and released by the National Center for Supercomputing Applications in 1993?

A dividend of high performance computing...

And now for something completely different...

Question: What historically significant web application was developed and released by the National Center for Supercomputing Applications in 1993?

Answer: The NCSA Mosaic Web Browser. This was the precursor of all browsers such as Netscape, Firefox, Safari, Chrome, etc.



Image source: http://www.ncsa.illinois.edu/Projects/images/mosaic_plaque.jpg

Some material used in creating these slides comes from

- Johnnie W. Baker, CS 4/59995 Parallel Programming, Kent State University
- Henry Neeman, University of Oklahoma Supercomputing Center
- Oak Ridge and Lawerance Livermore National Laboratories
- Lecture on history of supercomputing from 2009 offering of CMPE113 by Andrea Di Blas, University of California Santa Cruz.
- Wikipedia provided a starting point and led to many pages from on which facts and images were found.
- Don Becker: The Inside Story of the Beowulf Saga